SIA168 High-Side Measurement Current Shunt Monitor

1. General Description

The SIA168 is a high-side, unidirectional, current shunt monitor. Wide input common- mode voltage range, low quiescent current, and tiny SOT-23 packaging enable use in a variety of applications.

Input common-mode and power-supply voltages are independent and can range from 3.0V to 60 V. Quiescent current is only 50 μA, which permits connecting the power supply to either side of the current measurement shunt with minimal error.

The device converts a differential input voltage to a current output. This current is converted back to a voltage with an external load resistor that sets any gain from 1 to over 100. Although designed for current shunt measurement, the circuit invites creative applications in measurement and level shifting.

SIA168 available in SOT23-5 and specified for the –40°C to 125°C temperature range.

2. Application

- Current Shunt Measurement
- Motors, PC level shifting
- Battery Chargers
- Precision Current Source
- Drones

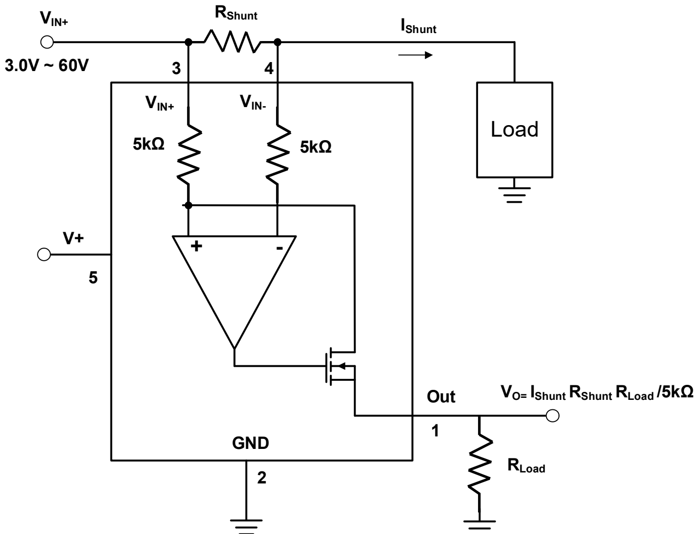
3. Feature

- Complete Unidirectional High-Side Current Measurement Circuit
- Wide Supply and Common-Mode Range; 3.0 V to 60 V
- Independent Supply and Input Common-Mode Voltages
- Single Resistor Gain Set
- Low Quiescent Current (50 μA Typical)
- Wide Temperature Range: –40°C to +125°C
- 5-Pin SOT-23 Package

4. Device Information

Part Number	Package	Body Size (NOM)
SIA168	SOT23-5	2.90mm × 1.60mm

Typical Application Circuit

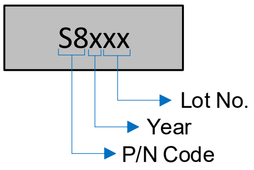


5. Ordering Information

Part Number	Marking	Operation Temperature	Package	Packing Form
SIA168	S8	-40°C ~ 125°C	SOT23-5	3000 pieces per reel

6. IC Marking Identification

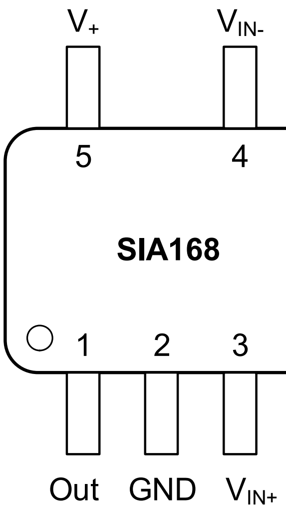
SOT23-5



7. Absolute Maximum Ratings

		MIN	MAX	UNIT
V+	Supply Voltage	–0.3	70	V
V_{IN}	Input Common-mode Voltage	–0.3	70	V
	Sense Voltage, V_{SENSE}=Input Differential Voltage, (V_{IN+})-(V_{IN-})	-10	10	V
	Input current into any pin		10	mA
T_A	Operating temperature	-40	125	°C
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	-65	125	°C

8. Pin Configuration and Functions



Pin Functions – SIA168			
Pin No.	**Name**	**I/O**	**Description`**
1	Out	Analog Output	Output current
2	GND	--	Ground
3	V_{IN+}	Analog Input	Positive input voltage
4	V_{IN-}	Analog Input	Negative input voltage
5	V_+	Analog Input	Power supply voltage

9. Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
V+	Power supply voltage	3.0	60	V
V_{CM}	Common-mode voltage	3.0	60	V
T_A	Operation temperature range	-40	125	°C

10. Thermal Information

PARAMETER		MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	250	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	81	°C/W

11. Electrical Characteristics

all characteristics at T_A=25°C, V+ =3.3V, V_{IN+}=12 V, V_{SENSE}=V_{IN+}-V_{IN-}=1mV, and R_L = 120kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input						
CMRR	Common-mode rejection ratio	V_{SENSE}=50mV, V_{IN+}=3V to 60V	90			dB
V_{OFFSET}	Offset voltage	T_A=25°C		±0.3	±1.8	mV
		T_A=-40°C to 125°C			±2.4	mV
$V_{OFFSET(TA)}$	Offset voltage vs temperature	T_A=-40°C to 125°C		1.5		μV/°C
I_B	Bias current	T_A=25°C		42		μA
		T_A=-40°C to 125°C			50	μA
Output						
	Transconductance vs temperature	V_{SENSE}=10mV to 150mV, T_A=25°C	196		204	μA/V
	Nonlinearity error	V_{SENSE}=10mV to 150mV			±0.1	%
	Total output error	V_{SENSE}=100mV, T_A=25°C			±2.5	%
		V_{SENSE}=100mV, T_A=-40°C to 125°C			±3.3	%
	Output capacitance			40		pF
	Swing to power supply, V+			(V+) +0.6		V
	Swing to V_{IN+}				V_{IN+}	V
Frequency Response						
	Bandwidth	R_{LOAD} =5kΩ		330		kHz
		R_{LOAD} =120kΩ		25		kHz
	Settling time	To 0.1%, R_{LOAD} =5kΩ		6		μs
		To 0.1%, R_{LOAD} =120kΩ		100		μs
Power Supply						
I_Q	Quiescent current	V_{SENSE}=100mV, T_A=25°C		50	60	μA

12. Typical Performance Characteristics

all characteristics at T_A=25°C, V_S =3.3V, V_{IN+}=12 V, and R_L = 120kΩ (unless otherwise noted)

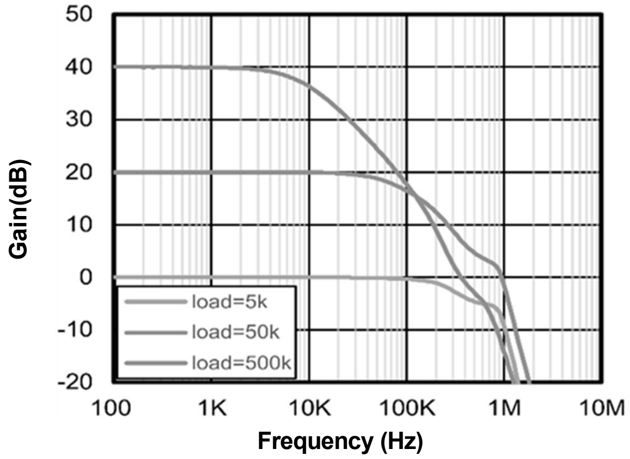


Figure 1: Gain vs. Frequency

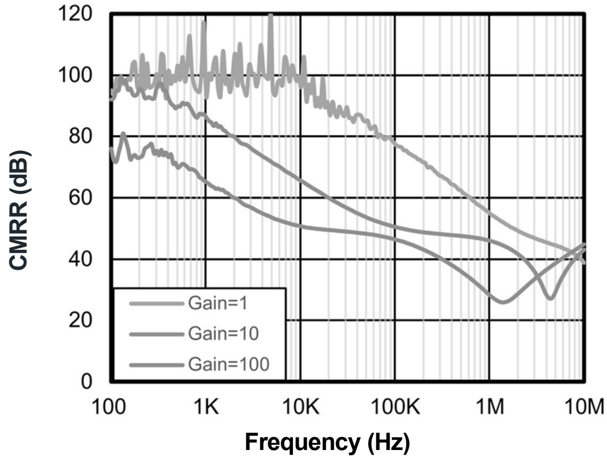


Figure 2: Common mode rejection vs. Frequency

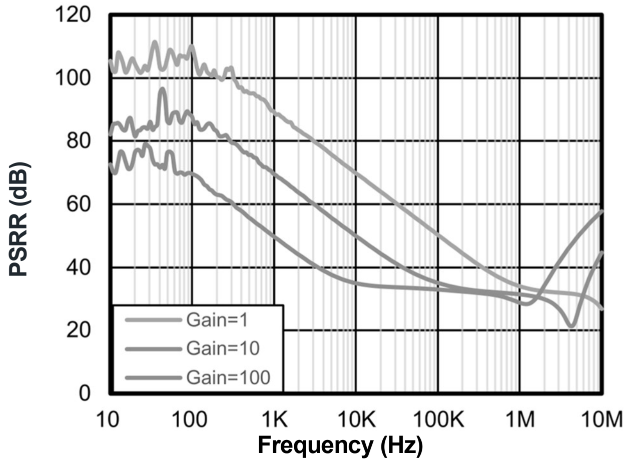


Figure 3: Power supply rejection vs. Frequency

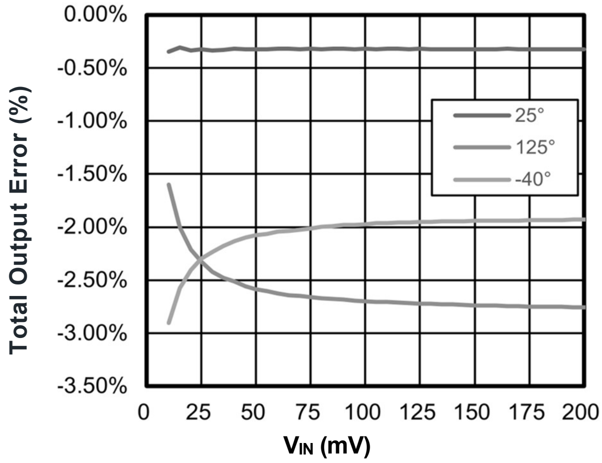


Figure 4: Total output error vs. V_{IN}(V_{IN}=V_{IN+}-V_{IN-})

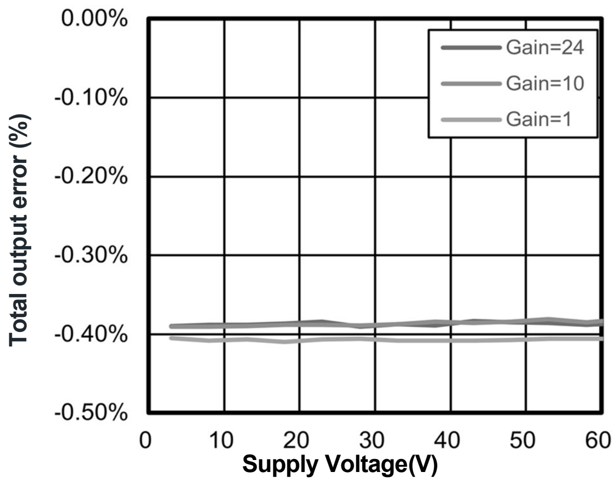


Figure 5: Total Output Error vs. Power-Supply Voltage

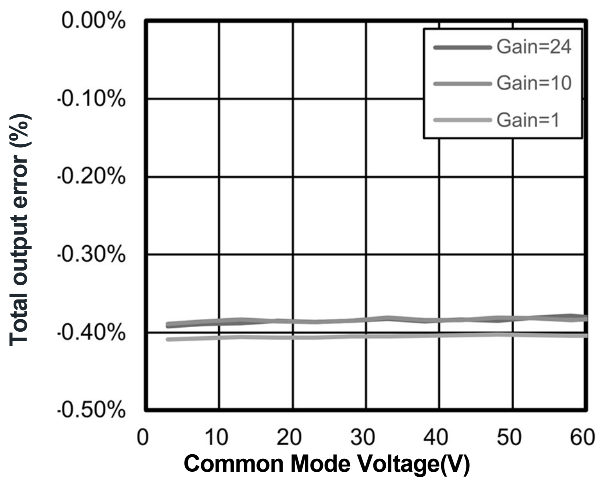


Figure 6: Total output Error vs. Common mode Voltage

13. Typical Performance Characteristics

all characteristics at T_A=25°C, V_S =3.3V, V_{IN+}=12 V, and R_L = 120kΩ (unless otherwise noted)

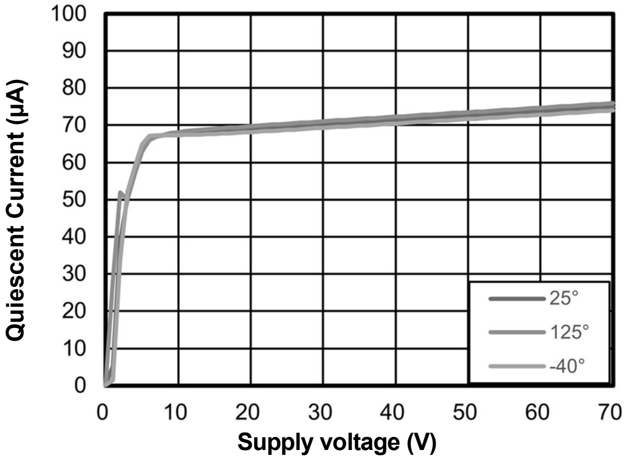


Figure 7: Quiescent Current vs. Supply voltage

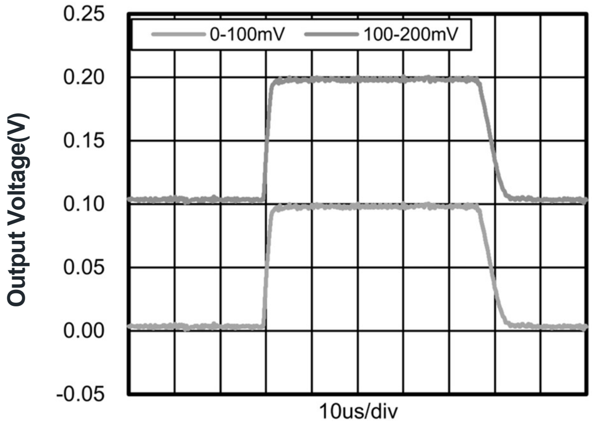


Figure 8: Step Response, Gain = 1

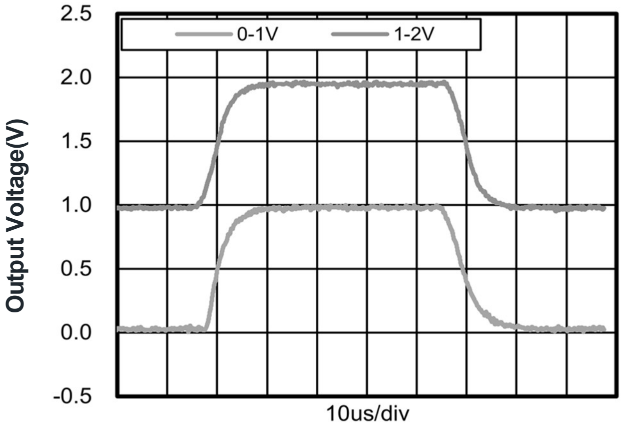


Figure 9: Step Response, Gain = 10

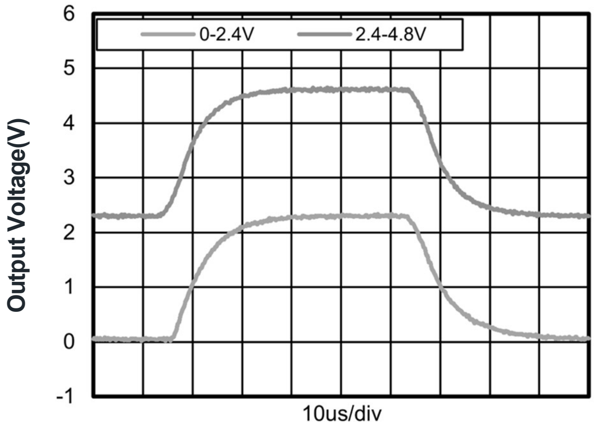


Figure 10: Step Response, Gain = 24

14. ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
		Charged-device model (CDM), per JEDEC specification	±1500	

(1) EDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

15. Function Block Diagram

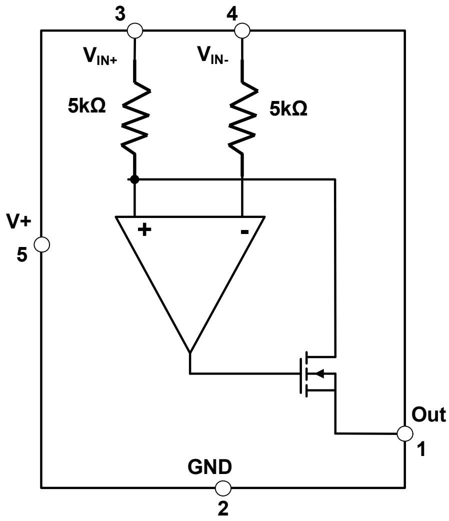


Figure 11. Functional Block Diagram

16. Feature Description

Output Range

The output voltage keeps linear in the specified range of the differential input voltage and the load resistor. When the differential input voltage is beyond the linear range, the output voltage reaches the maximum value. The maximum output voltage is limited by V_{IN+} and the power supply voltage. The relationship between maximum output voltage (V_{Out} max) and V_{IN+}, V+ depends on either Equation 1 or Equation 2, whichever is lower.

$$V_{Out}\ max = (V+) + 0.7\ V$$

$$V_{Out}\ max = V_{IN+}$$

Bandwidth

The bandwidth is related to the load resistor. Increase the load resistor to acquire higher gain, which means lower band width. There are several bandwidth curves in different load resistors in Figure 1. Note that the parasitic capacitance parallel to the load resistor forms a pole with the load resistor in frequency characteristics, which means bandwidth loss. Keep the parasitic capacitance low to get no loss in bandwidth.

17. Application Information

The SIA168 internal circuit is shown in Figure 12. The load current in applications flows through the shunt resistor and forms a voltage drop as the differential input voltage (V_{dm}) to the chip. V_{dm} is delivered to the voltage on R_{G1} (V_{RG1}) by the SIA168, causing a current flowing into the MOSFET. The load resistor converts this current to output voltage.

$$I_{Shunt} \cdot R_{Shunt} = V_{IN+} - V_{IN-}$$

$$I_{Load} = \frac{V_{IN+} - V_{IN-}}{R_{G1}} = g_m (V_{IN+} - V_{IN-})$$

Where $g_m = 1/R_{G1} = 200\mu A/V$.

The output voltage is shown in Equation 5.

$$V_{out} = I_{Load} \cdot R_{Load} = g_m \cdot (I_{Shunt} \cdot R_{Shunt}) \cdot R_{Load}$$

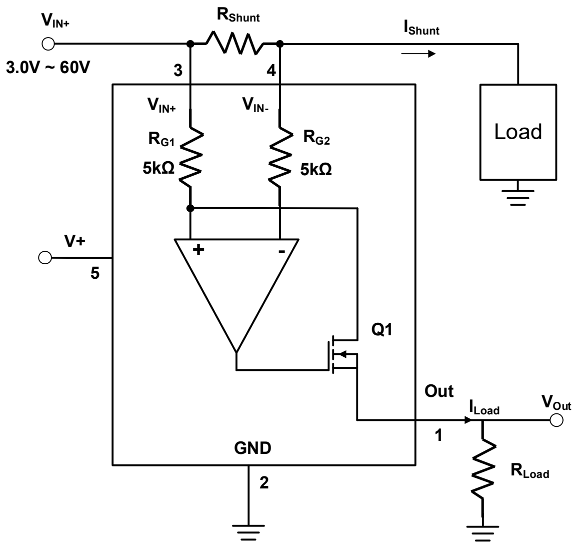


Figure 12. Internal circuit & Typical Application Circuit

Typical Application

Output Voltage Detection

An analog-to-digital converter (ADC) is commonly used in output voltage detections. The input impedance of ADCs is parallel to the load resistor. Considering that the output voltage is vulnerable to the load impedance, the effect of the input impedance of ADCs on the output voltage is not negligible. To eliminate such influence on the output voltage, a buffer between the ADCs input and load resistor is added to isolate these two parts. The connection between the SIA168 output and ADC is shown in Figure 13. If the output signal needs filtering, a capacitor is parallel to the load resistor to get an RC filter. The cut-off frequency is $1 / (2\pi R_{Load}C_{Load})$

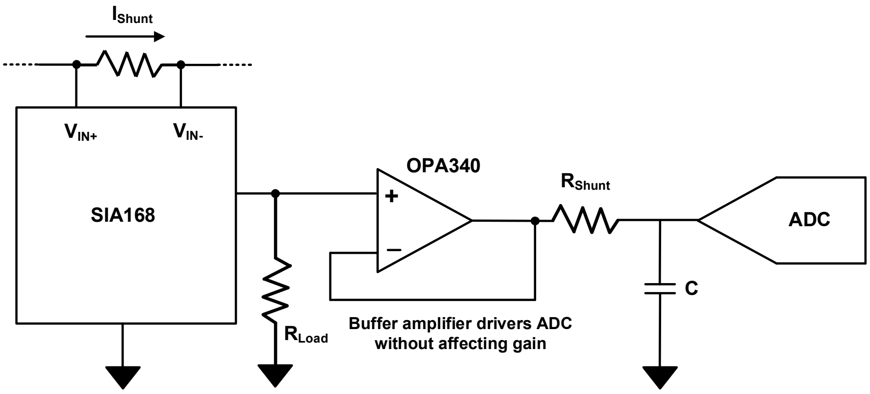


Figure 13. Buffer Output

Offsetting the Output Voltage

Some current sense amplifiers with the REF pin are used to set reference voltage. The SIA168 can realize such an offset function by a voltage divider on the output. Figure 14 illustrates the offset function circuit. The output voltage fluctuates above the offset voltage.

The offset voltage is shown below.

$$V_{Offset} = \frac{V_R R_2}{R_1 + R_2}$$

The equivalent load resistor is R1 parallel to R2. The output voltage is determined as below.

$$V_{out} = I_{Load} R_{Load} + V_{Offset} = I_{Load} \frac{R_1 R_2}{R_1 + R_2} + \frac{V_R R_2}{R_1 + R_2}$$

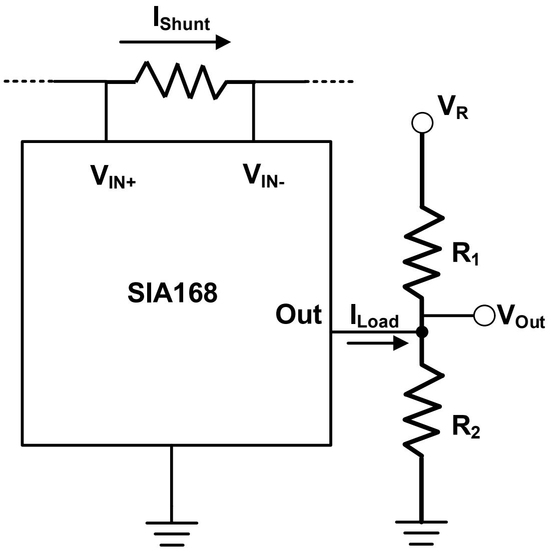
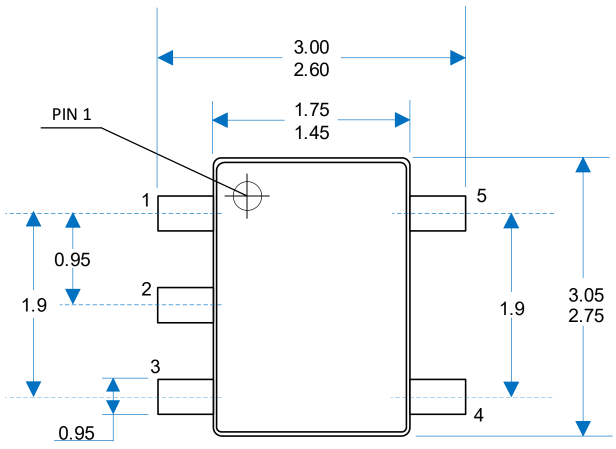


Figure 14. Offset Circuit

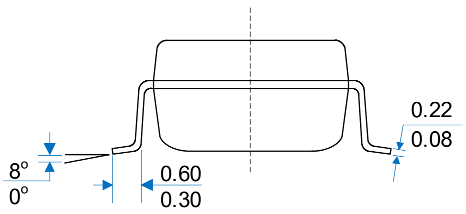
Power Supply Recommendations

To realize better noise decoupling performance on the power supply, the power supply bypass capacitor is placed as close as possible to the supply and the ground terminal. It’s recommended to use a 0.1μF capacitor. Additional bypass capacitors can get better noise suppression on the power supply.

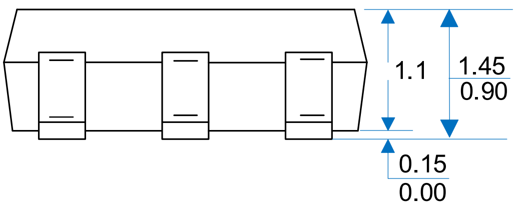
18. Package Outlines: SOT23-5



Top View



Side View 1



Side View 2

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