

Dual-Channel Digital Isolators

1. General Description

The SiS772x devices are high-performance dual-channel digital isolators. The SiS772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS digital I/O. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO₂) insulation barrier, and each channel input integrated Schmitt trigger to provide excellent noise immunity. The SiS772x features two channels transferring digital signals in one direction for applications such as isolated digital I/O.

The SiS7720 features two channels transferring digital signals in one direction for applications such as isolated digital I/O. The SiS7721 / SiS7722 devices have 2 channels with 1 channel in each direction, making them ideal for isolating the Tx and Rx lines of a transceiver, such as RS485, CAN, RS232 communication. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H.

2. Application

- BMS
- Industrial Automation
- Motor Control
- Isolated Power Supplies
- Solar Inverters
- Isolated SPI, RS485, CAN, RS232 etc

3. Feature

- Data rate: DC to 150Mbps
- Default output High (SiS772xH) and Low (SiS772xL) Options
- Power supply voltage: 2.5V to 5.5V
- 2.5V to 5.5V level translation
- CMTI :100kV/us
- Operation temperature: -40°C to +125°C
- Safety certifications:
- HBM 8KV ESD Rating
- 3750V_{RMS} isolation for SOIC-8 package
- 5000V_{RMS} isolation for SOIC-8W package

4. Device Information

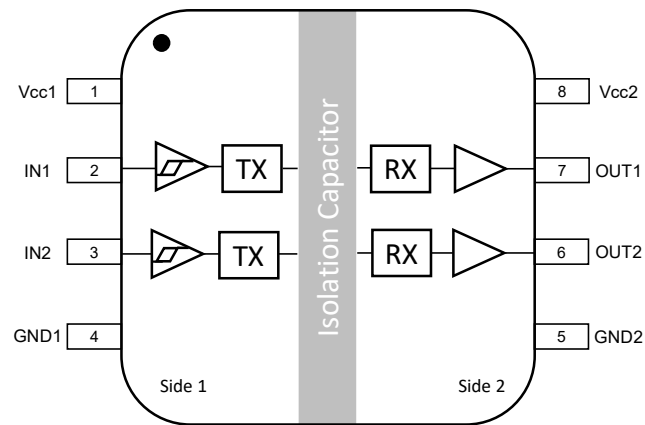
Part Number	Package	Body Size (NOM)
SiS7720	S: SOP8	4.90mm × 3.90mm
SiS7721	G: SOW8	5.85mm × 7.50mm
SiS7722		

5. Ordering Information

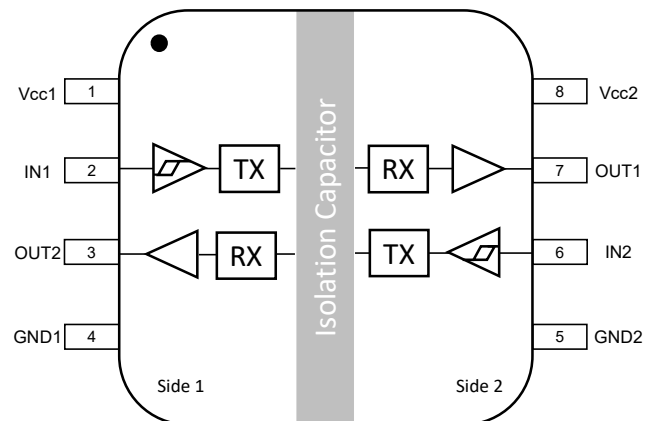
Part Number	Marking	Input Channel	Output Channel	Default Output	Isolation Rating(kV _{RMS})	Package	Packing Form
SiS7720HS	iS7720HS	2	0	High	3.75	SOP8	3000 pieces per reel
SiS7721HS	iS7721HS	1	1	High			
SiS7722HS	iS7722HS	1	1	High			
SiS7720LS	iS7720LS	2	0	Low			
SiS7721LS	iS7721LS	1	1	Low			
SiS7722LS	iS7722LS	1	1	Low			
SiS7720HG	iS7720HG	2	0	High	5.0	SOW8	1000 pieces per reel
SiS7721HG	iS7721HG	1	1	High			
SiS7722HG	iS7722HG	1	1	High			
SiS7720LG	iS7720LG	2	0	Low			
SiS7721LG	iS7721LG	1	1	Low			
SiS7722LG	iS7722LG	1	1	Low			

6. Pin Configuration and Functions

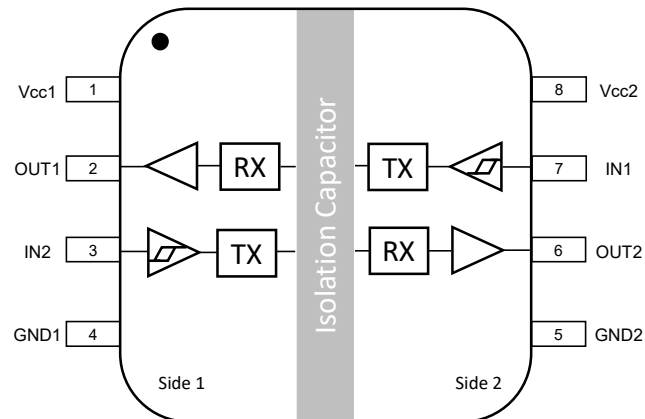
SiS7720 SOIC-8 / SOIC-8W Top View



SiS7721 SOIC-8 / SOIC-8W Top View



SiS7722 SOIC-8 / SOIC-8W Top View



Pin Functions – SiS7720/SiS7721/SiS7722				
SiS7720H SiS7720L	SiS7721H SiS7721L	SiS7722H SiS7722L	Name	Description
1	1	1	Vcc1	Power supply for Side 1.
2	2	7	IN1	Digital input 1 on Side 1/Side 2, corresponds to logic output 1 on Side 2/Side 1.
3	6	3	IN2	Digital input 2 on Side 1/Side 2, corresponds to logic output 2 on Side 2/Side 1.
4	4	4	GND1	Ground, Side 1.
5	5	5	GND2	Ground, Side 2.
6	3	6	OUT2	Digital output 2 on Side 2/Side 1, OUT2 is the logic output for the IN2 input on Side 1/Side 2.
7	7	2	OUT1	Digital output 1 on Side 1/Side 2, OUT1 is the logic output for the IN1 input on Side 1/Side 2.
8	8	8	Vcc2	Power supply for Side 2.

7. Absolute Maximum Ratings

Parameter		Min.	Max.	Unit
Vcc1, Vcc2	Supply Voltage	−0.5	+6.0	V
V _{IN1} , V _{IN2}	Input Voltage	−0.5	Vcc1 + 0.5	
OUT1, OUT2	Output Voltage	−0.5	Vcc2 + 0.5	
T _{J(MAX)}	Maximum junction temperature	−40	150	°C
T _{stg}	Storage temperature	−40	150	°C

8. Recommended Operating Conditions

Parameter		Min.	Max.	Unit.
Vcc1, Vcc2	Supply voltage	2.5	5.5	V
T _A	Ambient temperature	−45	125	°C

9. Electrical Characteristics---5V Supply

V_{cc1}=5V±10%, V_{cc2}=5V±10%, T_A=25°C (over recommended operating conditions, unless otherwise noted)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{OH} High-level output voltage	I _{OH} =-4 mA	V _{cco} ^① -0.4	V _{cco} -0.2		V
V _{OL} Low-level output voltage	I _{OL} = 4 mA		0.2	0.4	V
V _{IH} Logic input high level threshold	V _{CCI} =V _{cc2} =5.0V	2.0			V
V _{IL} Logic input low level threshold	V _{CCI} =V _{cc2} =5.0V			0.8	V
I _{IN} Input current	0≤V _{IN1} , V _{IN2} ≤5V	-20		20	uA
SiS7720 Supply Current					
Supply current -- DC signal					
I _{cc1} I _{cc2}	V _{cc1} =V _{cc2} =5.5V V _{IN} =5.5V (SiS7720H), V _{IN} =GND (SiS7720L)		1.4 1.8	2.5 4.0	mA
I _{cc1} I _{cc2}	V _{cc1} =V _{cc2} =5.5V V _{IN} =GND (SiS7720H), V _{IN} =5.5V (SiS7720L)		4.7 2.0	8.5 4.5	mA
Supply current – AC signal					
1Mbps					
I _{cc1} I _{cc2}	500kHz logic Frequency		3.0 2.0	5.6 4.4	mA
10Mbps					
I _{cc1} I _{cc2}	5MHz logic Frequency		3.1 2.5	6.0 6.8	mA
150Mbps					
I _{cc1} I _{cc2}	75MHz logic Frequency		3.7 10.7	7.0 38	mA
SiS7721 Supply Current					
Supply current -- DC signal					
I _{cc1} I _{cc2}	V _{cc1} =V _{cc2} =5.5V V _{IN} =5.5V (SiS7721H), V _{IN} =GND (SiS7721L)		2.0 2.0	4.0 4.0	mA
I _{cc1} I _{cc2}	V _{cc1} =V _{cc2} =5.5V V _{IN} =GND (SiS7721H), V _{IN} =5.5V (SiS7721L)		3.7 3.7	7.0 7.0	mA
Supply current – AC signal					
1Mbps					
I _{cc1} I _{cc2}	500kHz logic Frequency		2.9 2.9	5.6 5.6	mA
10Mbps					

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Icc1	5MHz logic Frequency		3.2	6.8	mA
Icc2			3.2	6.8	
150Mbps					
Icc1	75MHz logic Frequency		7.5	25	mA
Icc2			7.5	25	
SiS7722 Supply Current					
Supply current -- DC signal					
Icc1	Vcc1=Vcc2=5.5V VIN=5.5V (SiS7722H), VIN=GND (SiS7722L)		2.0	4.0	mA
Icc2			2.0	4.0	
Icc1	Vcc1=VCC2=5.5V VIN=GND (SiS7722H), VIN=5.5V (SiS7722L)		3.7	7.0	mA
Icc2			3.7	7.0	
Supply current – AC signal					
1Mbps					
Icc1	500kHz logic Frequency		2.9	5.6	mA
Icc2			2.9	5.6	
10Mbps					
Icc1	5MHz logic Frequency		3.2	6.8	mA
Icc2			3.2	6.8	
150Mbps					
Icc1	75MHz logic Frequency		7.5	25	mA
Icc2			7.5	25	

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWmin	$C_L=15\text{pF}$	6.67			ns
PWD Pulse width distortion $ t_{\text{PHL}} - t_{\text{PLH}} $	$C_L=15\text{pF}$			6	ns
DR Data Rate	$C_L=15\text{pF}$	0		150	Mbps
$t_{\text{PLH}}, t_{\text{PHL}}$ Propagation Delay Time	$C_L=15\text{pF}$			26	ns
$t_{\text{sk}}(\text{CD})$ Channel-to-channel Output Skew Time ¹	Same direction channels			3.6	ns
$t_{\text{sk}}(\text{OD})$ Channel-to-channel Output Skew Time ¹	Reverse direction channels			3.6	ns
SiS772xH Output Voltage	$V_{\text{CC1}}=V_{\text{CC2}}=5.0\text{V}$, Input is open	4.5	5	5.5	V
SiS772xL Output Voltage	$V_{\text{CC1}}=V_{\text{CC2}}=5.0\text{V}$, Input is open	-0.5	0	0.5	V
CMTI Common-mode Transient Immunity	$C_L=15\text{pF}$	100			kV/us

^① V_{CC1} = Input-side V_{CC} ; V_{CC0} = Output-side V_{CC} .

10. Electrical Characteristics---3.3V Supply

Vcc1=3.3V±10%, Vcc2=3.3V±10%, T_A=25°C (over recommended operating conditions, unless otherwise noted)

Parameter		Test Conditions	Mni.	Typ.	Max.	Unit
Side 1 (ONLY)						
V _{OH}	High-level output voltage	I _{OH} =-4 mA	V _{cco} -0.4	V _{cco} -0.2		V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA		0.2	0.4	V
V _{IH}	Logic input high level threshold	V _{cc} 1=V _{cc} 2=3.3V	2.0			V
V _{IL}	Logic input low level threshold	V _{cc} 1=V _{cc} 2=3.3V			0.8	V
I _{IN}	Input current	0≤V _{IN1} , V _{IN2} ≤5V	-20		20	uA
SiS7720 Supply Current						
Supply current -- DC signal						
I _{cc} 1		V _{cc} 1=V _{cc} 2=3.6V V _{IN} =3.6V (SiS7720H), V _{IN} =GND (SiS7720L)		1.3	2.5	mA
I _{cc} 2				1.7	4.0	
I _{cc} 1		V _{cc} 1=V _{cc} 2=3.6V V _{IN} =GND (SiS7720H), V _{IN} =3.6V (SiS7720L)		4.7	8.5	mA
I _{cc} 2				1.9	4.5	
Supply current – AC signal						
1Mbps						
I _{cc} 1		500kHz logic Frequency		3.0	5.6	mA
I _{cc} 2				1.9	4.4	
10Mbps						
I _{cc} 1		5MHz logic Frequency		3.0	6.0	mA
I _{cc} 2				2.3	5.7	
150Mbps						
I _{cc} 1		75MHz logic Frequency		3.6	6.9	mA
I _{cc} 2				8.6	26	
SiS7721 Supply Current						
Supply current -- DC signal						
I _{cc} 1		V _{cc} 1=V _{cc} 2=3.6V V _{IN} =3.6V (SiS7721H), V _{IN} =GND (SiS7721L)		1.9	4.0	mA
I _{cc} 2				1.9	4.0	
I _{cc} 1		V _{cc} 1=V _{cc} 2=3.6V V _{IN} =GND (SiS7721H), V _{IN} =3.6V (SiS7721L)		3.6	7.0	mA
I _{cc} 2				3.6	7.0	
Supply current – AC signal						
1Mbps						

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Icc1 Icc2	500kHz logic Frequency		2.8 2.8	5.6 5.6	mA
10Mbps					
Icc1 Icc2	5MHz logic Frequency		3.1 3.1	6.1 6.1	mA
150Mbps					
Icc1 Icc2	75MHz logic Frequency		6.4 6.4	18.5 18.5	mA
SiS7722 Supply Current					
Supply current -- DC signal					
Icc1 Icc2	Vcc1=Vcc2=3.6V VIN=3.6V (SiS7722H), VIN=GND (SiS7722L)		1.9 1.9	4.0 4.0	mA
Icc1 Icc2	Vcc1=Vcc2=3.6V VIN=GND (SiS7722H), VIN=3.6V(SiS7722L)		3.6 3.6	7.0 7.0	
Supply current – AC signal					
1Mbps					
Icc1 Icc2	500kHz logic Frequency		2.8 2.8	5.6 5.6	mA
10Mbps					
Icc1 Icc2	5MHz logic Frequency		3.1 3.1	6.1 6.1	mA
150Mbps					
Icc1 Icc2	75MHz logic Frequency		6.4 6.4	18.5 18.5	mA

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWmin	$C_L=15\text{pF}$	6.67			ns
PWD Pulse width distortion ($t_{\text{PHL}} - t_{\text{PLH}}$)	$C_L=15\text{pF}$			6	ns
DR Data Rate	$C_L=15\text{pF}$	0		150	Mbps
$t_{\text{PLH}}, t_{\text{PHL}}$ Propagation Delay Time	$C_L=15\text{pF}$	5		26	ns
$\text{tsk}_{(\text{CD})}$ Channel-to-channel Output Skew Time ¹	Same direction channels			3.6	ns
$\text{tsk}_{(\text{OD})}$ Channel-to-channel Output Skew Time ¹	Reverse direction channels			3.6	ns
CMTI Common-mode Transient Immunity	$C_L=15\text{pF}$	100			kV/us

11. Electrical Characteristics---2.5V Supply

Vcc1=2.5V±10%, Vcc2=2.5V±10%, T_A=25°C (over recommended operating conditions, unless otherwise noted)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Side 1 (ONLY)					
V _{OH} High-level output voltage	I _{OH} = -4 mA	V _{CCO} -0.4	V _{CC} -0.2		V
V _{OL} Low-level output voltage	I _{OL} = 4 mA		0.2	0.4	V
V _{IH} Logic input high level threshold	V _{CC1} =V _{CC2} =2.5V	2.0			V
V _{IL} Logic input low level threshold	V _{CC1} =V _{CC2} =2.5V			0.8	V
I _{IN} Input current	0 ≤ V _{IN1} , V _{IN2} ≤ 5V	-20		20	uA
SiS7720 Supply Current					
Supply current -- DC signal					
I _{CC1} I _{CC2}	V _{CC1} =V _{CC2} =2.5V V _{IN} =2.5V (SiS7720H), V _{IN} =GND (SiS7720L)		1.3 1.7	2.5 4.0	mA
I _{CC1} I _{CC2}	V _{CC1} =V _{CC2} =2.5V V _{IN} =GND (SiS7720H), V _{IN} =2.5V (SiS7720L)		4.6 1.9	8.5 4.5	mA
Supply current – AC signal					
1Mbps					
I _{CC1} I _{CC2}	500kHz logic Frequency		3.0 1.9	5.6 4.4	mA
10Mbps					
I _{CC1} I _{CC2}	5MHz logic Frequency		3.0 2.1	5.3 5.2	mA
150Mbps					
I _{CC1} I _{CC2}	75MHz logic Frequency		3.6 7.0	6.7 20	mA
SiS7721 Supply Current					
Supply current -- DC signal					
I _{CC1} I _{CC2}	V _{CC1} =V _{CC2} =2.5V V _{IN} =2.5V (SiS7721H), V _{IN} =GND (SiS7721L)		1.9 1.9	4.0 4.0	mA
I _{CC1} I _{CC2}	V _{CC1} =V _{CC2} =2.5V V _{IN} =GND (SiS7721H), V _{IN} =2.5V (SiS7721L)		3.6 3.6	7.0 7.0	mA
Supply current – AC signal					
1Mbps					
I _{CC1} I _{CC2}	500kHz logic Frequency		2.7 2.7	5.6 5.6	mA

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
10Mbps					
lcc1 lcc2	5MHz logic Frequency		2.9 2.9	5.8 5.8	mA
150Mbps					
lcc1 lcc2	75MHz logic Frequency		5.5 5.5	15 15	mA
SiS7722 Supply Current					
Supply current -- DC signal					
lcc1 lcc2	V _{cc1} =V _{cc2} =2.5V V _{IN} =2.5V (SiS7722H), V _{IN} =GND (SiS7722L)		1.9 1.9	4.0 4.0	mA
lcc1 lcc2	V _{cc1} =V _{cc2} =2.5V V _{IN} =GND (SiS7722H), V _{IN} =2.5V (SiS7722L)		3.6 3.6	7.0 7.0	mA
Supply current – AC signal					
1Mbps					
lcc1 lcc2	500kHz logic Frequency		2.7 2.7	5.6 5.6	mA
10Mbps					
lcc1 lcc2	5MHz logic Frequency		2.9 2.9	5.8 5.8	mA
150Mbps					
lcc1 lcc2	75MHz logic Frequency		5.5 5.5	15 15	mA

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWmin	$C_L=15\text{pF}$	6.67			ns
PWD Pulse width distortion ($t_{\text{PHL}} - t_{\text{PLH}}$)	$C_L=15\text{pF}$			6	ns
DR Data Rate	$C_L=15\text{pF}$	0		150	Mbps
$t_{\text{PLH}}, t_{\text{PHL}}$ Propagation Delay Time	$C_L=15\text{pF}$	5		28	ns
$t_{\text{sk}}(\text{CD})$ Channel-to-channel Output Skew Time ¹	Same direction channels			3.6	ns
$t_{\text{sk}}(\text{OD})$ Channel-to-channel Output Skew Time ¹	Reverse direction channels			3.6	ns
CMTI Common-mode Transient Immunity	$C_L=15\text{pF}$	100			kV/us

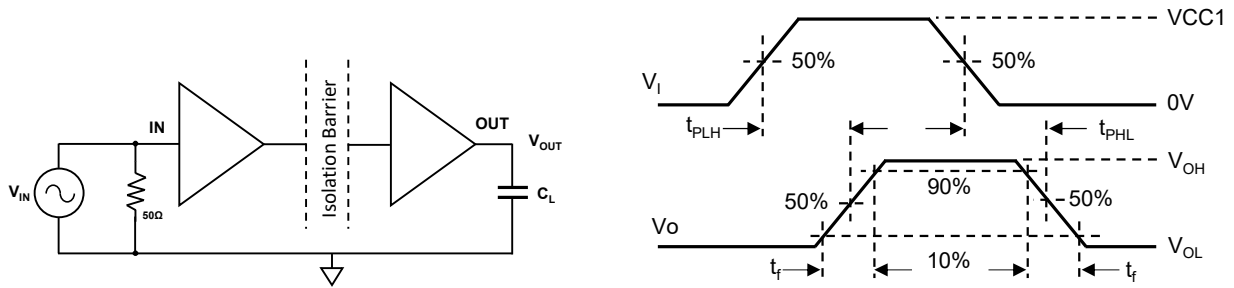
12. Thermal Information

Thermal Metric	S(SOP8)	G(SOW8)	Unit
$R_{\theta\text{JA}}$ Junction-to-ambient thermal resistance	110	92.5	°C/W

13. ESD Ratings and V_{ISO}

Parameter	Test Conditions	Value		Unit
		S	G	
$V_{\text{(ESD)}}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pins	±8000	V
		All pins	±4000	
	Charged-device model (CDM), per JEDEC specification		±2000	
	Machine Model JEDEC JESD22-A115-A, all pins		±200	
V_{ISO} Withstand isolation voltage	$V_{\text{TEST}} = V_{\text{ISO}} = 2500 V_{\text{RMS}}, t = 60 \text{ s (qualification)}; V_{\text{TEST}} = 1.2 \times V_{\text{ISO}} = 3000 V_{\text{RMS}}, t = 1 \text{ s (100\% production)}$	3750	5000	V_{RMS}

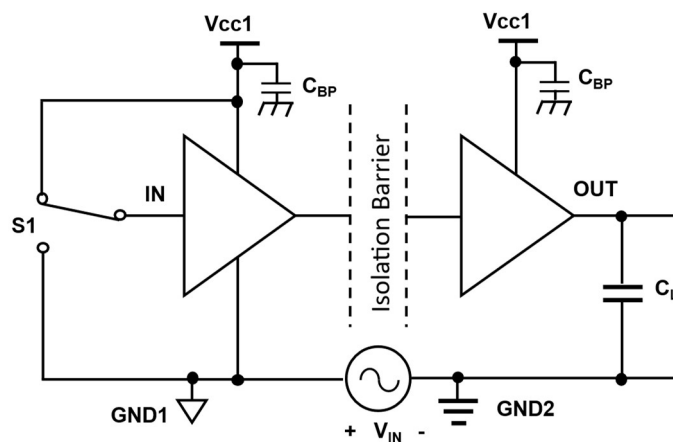
14. Parameter Measurement Information



Switching Characteristics Test Circuit and Voltage Waveforms

Notes:

1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_o = 50\Omega$. At the input, 50Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
2. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.



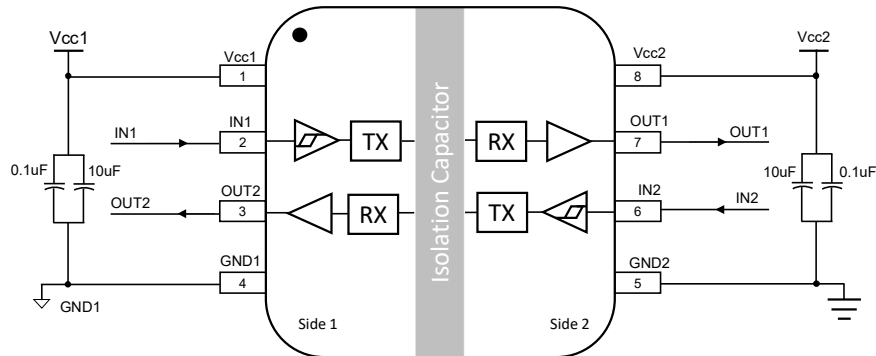
• Common-Mode Transient Immunity Test Circuit

Notes:

1. The High Voltage Surge Generator generates repetitive surges with > 1 kV, < 10 ns rise time and fall time to reach common-mode transient noise with > 100 kV/ μ s slew rate.
2. $C_L = 15$ pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: The output must remain stable whenever the high voltage surges occurs.
4. C_{BP} is bypass capacitor, $0.1\mu F \sim 1\mu F$.

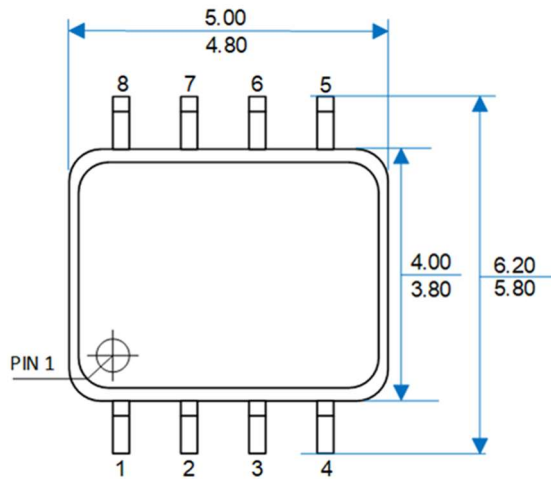
15. Typical Application

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the SiS772x devices only require two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass Vcc1 and Vcc2 pins with 0.1μF low-ESR ceramic capacitors and parallel and 10μF capacitor to GND1 and GND2, respectively. Place the bypass capacitors as close to the power supply input pins as possible.

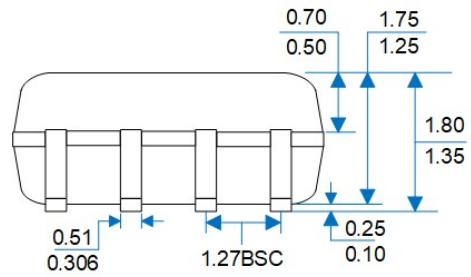


• **Typical Application Circuit of SiS772x**

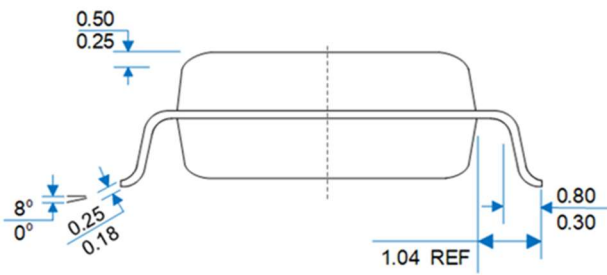
16. Package Outlines: SOP8



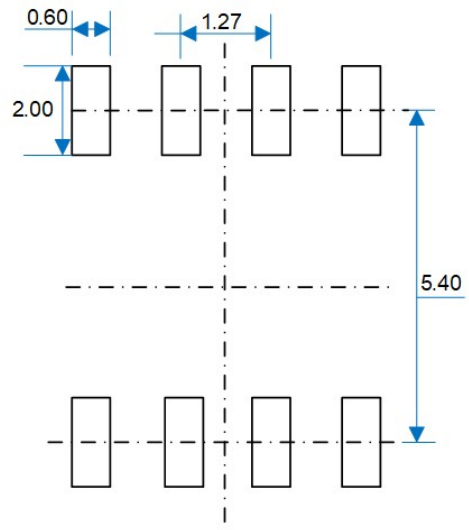
Top View



Side View 1

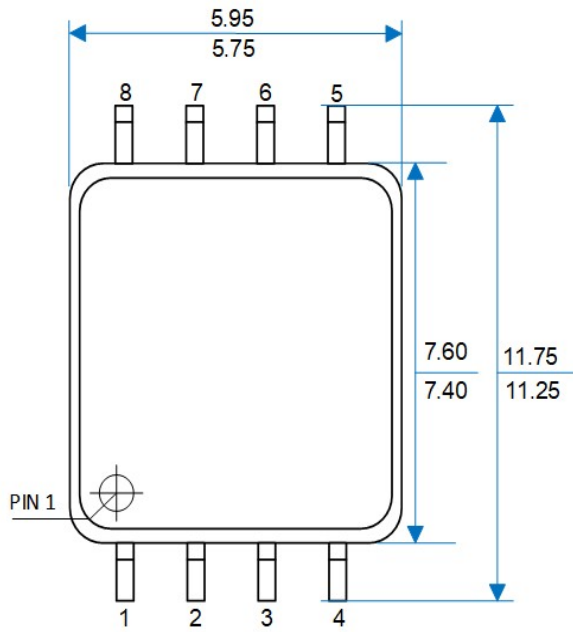


Side View 2

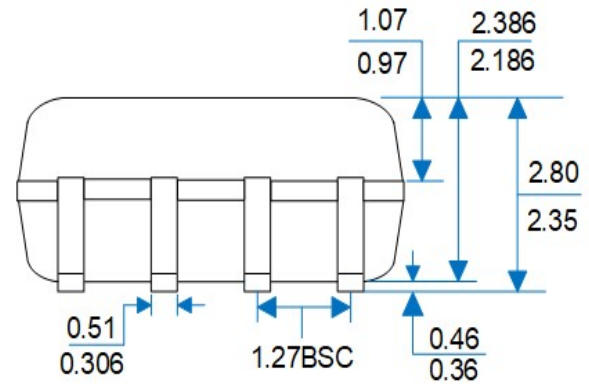


Recommended Land Pattern

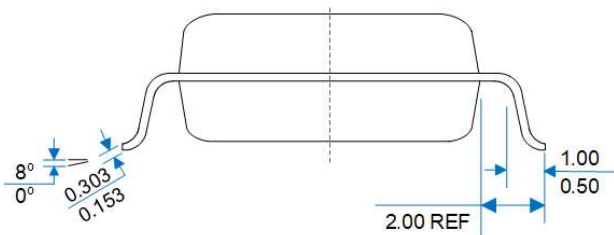
17. Package Outlines: SOW8



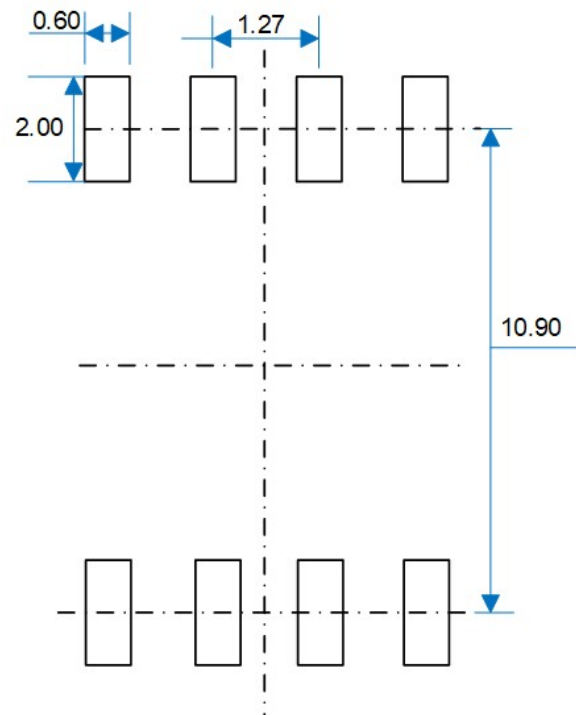
Top View



Side View 1



Side View 2



Recommended Land Pattern

Disclaim

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