Bidirectional I²C Isolators

1. General Description

The SiS154x devices are high reliability bidirectional isolators that are compatible with I²C interface. The SiS154x devices are safety, insulations withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The I²C clock of the SiS154x is up to 1MHz, and the common-mode transient immunity (CMTI) is up to 150kV/us. Wide supply voltage of the SiS154x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhances reliability and stability of use.

2. Application

- Power over Ethernet
- level shifting
- SMBus, or PMBus interface
- Isolated I²C buses
- Power over Ethernet
- BMS

3. Feature

- Bidirectional communication
- Open Drain Output
- With 3.5-mA Side 1 and 30- mA Side 2 sink current capability
- I²C Clock rate: up to 1MHz
- Hot swap protection
- Power supply voltage: 3.0V to 5.5V
- Support different supply voltage in primary side and secondary side.
- CMTI :100kV/us
- Operation temperature: –40°C to +125°C
- Safety certifications:
- 3.75kV$_{RMS}$ isolation for SOP8 package
- 5kV$_{RMS}$ isolation for SOW8 package

4. Device Information

Part Number	Package	Body Size(NOM)
SiS1540S	(S) SOP8	4.90mm × 3.90mm
SiS1541S		
SiS1540G	(G) SOW8	5.85mm × 7.50mm
SiS1541G		

5. Ordering Information

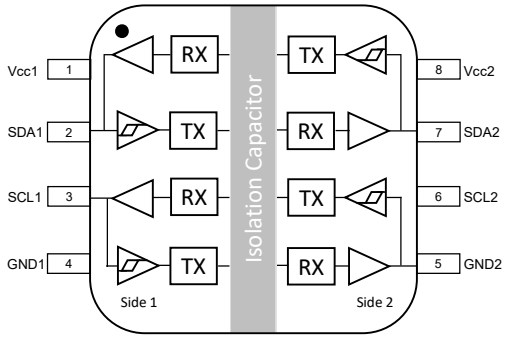
Part Number	Marking	Bidirectional Channel	Unidirectional Channel	Isolation Rating(kV$_{RMS}$)	Package	Packing Form
SiS1540S	iS1540S	2	0	3.75	SOP8	3000 pieces per reel
SiS1541S	iS1541S	1	1			
SiS1540G	iS1540G	2	0	5.0	SOW8	1000 pieces per reel
SiS1541G	iS1541G	1	1			

6. Absolute Maximum Ratings

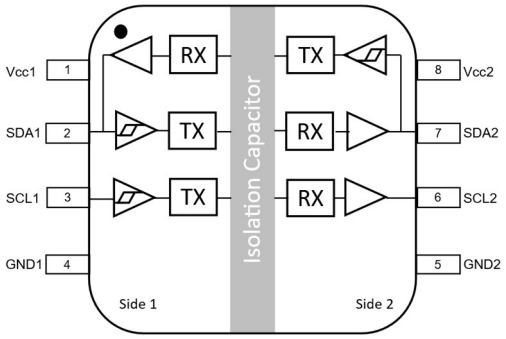
			MIN	MAX	UNIT
Voltage		Vcc1, Vcc2	–0.5	+6.0	V
		SDA1, SCL1	–0.5	Vcc1 + 0.5(3)	
		SDA2, SCL2	–0.5	Vcc2 + 0.5(3)	
I_O	Output current	SDA1, SCL1	–18	18	mA
		SDA2, SCL2	–100	100	
$T_{J(MAX)}$	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–40	150	°C

7. Pin Configuration and Functions

SiS1540 SOIC-8 / SOIC-8W Top View



SiS1541 SOIC-8 / SOIC-8W Top View



Pin Functions -- SiS1540		
Pin No.	**Name**	**Description`**
1	Vcc1	Supply voltage, side1
2	SDA1	Serial date input / output, side 1
3	SCL1	Serial clock input / output, side 1
4	GND1	Ground, side 1
5	GND2	Ground, side 2
6	SCL2	Serial clock input / output, side 2
7	SDA2	Serial date input / output, side 2
8	Vcc2	Supply Voltage, side 2

Pin Functions -- SiS1541		
Pin No.	**Name**	**Description**
1	Vcc1	Supply voltage, side1
2	SDA1	Serial date input / output, side 1
3	SCL1	Serial clock input, side 1
4	GND1	Ground, side 1
5	GND2	Ground, side 2
6	SCL2	Serial clock output, side 2
7	SDA2	Serial date input / output, side 2
8	Vcc2	Supply Voltage, side 2

8. Recommended Operating Conditions

		MIN	MAX	UNIT
Vcc1, Vcc2	Supply voltage	3.0	5.5	V
V_{SDA1}, V_{SCL1}	Input and output signal voltages, side 1	0	Vcc1	V
V_{SDA2}, V_{SCL2}	Input and output signal voltages, side 2	0	Vcc2	V
V_{IL1}	Low-level input voltage, side 1	0	0.5	V
V_{IH1}	High-level input voltage, side 1	0.7 × Vcc1	Vcc1	V
V_{IL2}	Low-level input voltage, side 2	0	0.3 × Vcc2	V
V_{IH2}	High-level input voltage, side 2	0.7 × Vcc2	Vcc2	V
I_{OL1}	Output current, side 1	0.5	3	mA
I_{OL2}	Output current, side 2	0.5	30	mA
CL1	Capacitive load, side 1		40	pF
CL2	Capacitive load, side 2		400	pF
T_A	Ambient temperature	–40	125	°C

9. Electrical Characteristics

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SIDE 1 (ONLY)						
V_{ILT1}	Voltage input threshold low, SDA1 and SCL1		500		700	mV
V_{IHT1}	Voltage input threshold high, SDA1 and SCL1		500		700	mV
V_{HYST1}	Voltage input hysteresis	$V_{IHT1} – V_{ILT1}$	50			mV
V_{OL1}	Low-level output voltage, SDA1 and SCL1 (1)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.0 mA	600		900	mV
ΔV_{OIT1}	Low-level output voltage to high level input voltage threshold difference, SDA1 and SCL1 (1)(2)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.0 mA	50			mV
SIDE 2 (ONLY)						
V_{ILT2}	Voltage input threshold low, SDA2 and SCL2				0.3 × Vcc2	V
V_{IHT2}	Voltage input threshold high, SDA2 and SCL2		0.7 × Vcc2			V
V_{OL2}	Low-level output voltage, SDA2 and SCL2	0.5 mA ≤ (I_{SDA2} and I_{SCL2}) ≤ 35 mA			0.4	V
BOTH SIDES						
$\|I_L\|$	Input leakage currents, SDA1, SCL1, SDA2, and SCL2	V_{SDA1}, V_{SCL1} = Vcc1; V_{SDA2}, V_{SCL2} = Vcc2		0.01	10	μA
Icc1	Supply current, side 1	4.5 V ≤ Vcc1, Vcc2 ≤ 5.5 V			12	mA
Icc2	Supply current, side 2	4.5 V ≤ Vcc1, Vcc2 ≤ 5.5 V			12	mA
Icc1	Supply current, side 1	3.0V ≤ Vcc1, Vcc2 ≤ 3.6V,			12	mA
Icc2	Supply current, side 2	3.0V ≤ Vcc1, Vcc2 ≤ 3.6V,			12	mA
CMTI	Common-mode transient immunity	$\|CM_H\|$ $\|CM_L\|$	25	35		kV/us

10. Thermal Information

THERMAL METRIC		S(SOP8)	G(SOW8)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	92.5	°C/W

11. Switching Characteristics

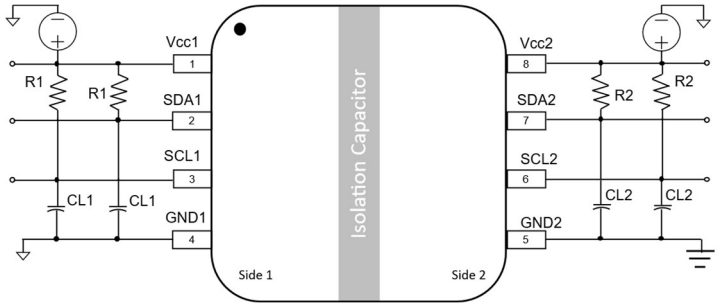
over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency						1000	kHz
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	R1 = 1.6kΩ, C1 = 40 pF	0.9 × Vcc1 to 900 mV		14	120	ns
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	R2 = 180 Ω, C2 = 400 pF	0.9× Vcc2 to 0.1 × Vcc2		30	120	ns
3.0V≤Vcc1, Vcc2≤3.6V							
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	R1 = 1.0kΩ, C1 = 40 pF	0.9 × Vcc1 to 900 mV		14	120	ns
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	R2 = 120 Ω, C2 = 400 pF	0.9× Vcc2 to 0.1 × Vcc2		32	120	ns
PROPAGATION DELAY							
t_{PLH1-2}	Low-to-High Propagation Delay, Side 1 to Side 2	4.5V ≤ Vcc1, Vcc2 ≤ 5.5V, R1 = 1.6kΩ, R2 = 180Ω, C1 = C2 = 0pF	0.5 × Vcc1 to 3.5V		48	130	ns
t_{PHL1-2}	High-to-Low Propagation Delay, Side 1 to Side 2		0.5 × Vcc1 to 0.4 V		50	275	ns
PWD_{1-2}	Pulse Width Distortion $\lvert t_{PLH1-2} - t_{PHL1-2} \rvert$				30	145	ns
t_{PLH2-1} (1)	Low-to-High Propagation Delay, Side 2 to Side 1		0.4 × Vcc2 to 0.7 × Vcc1		63	130	ns
t_{PHL2-1} (1)	High-to-Low Propagation Delay, Side 2 to Side 1		0.4 × Vcc2 to 0.9 V		18	155	ns
PWD_{2-1} (1)	Pulse Width Distortion $\lvert t_{PLH2-1} - t_{PHL2-1} \rvert$				54	85	ns
t_{PLH1-2}	Low-to-High Propagation Delay, Side 1 to Side 2	3.0V ≤ Vcc1, Vcc2 ≤ 3.6V, R1 = 1.0kΩ, R2 = 120Ω, C1 = C2 = 0pF	0.50 × Vcc2 to 0.7 × Vcc2		65	125	ns
t_{PHL1-2}	High-to-Low Propagation Delay, Side 1 to Side 2		0.70 to 0.4V		67	340	ns
PWD_{1-2}	Pulse Width Distortion $\lvert t_{PLH1-2} - t_{PHL1-2} \rvert$				25	215	ns
t_{PLH2-1} (1)	Low-to-High Propagation Delay, Side 2 to Side 1		0.50 × Vcc2 to 0.7 × Vcc1		68	130	ns
t_{PHL2-1} (1)	High-to-Low Propagation Delay, Side 2 to Side 1				23	210	ns
PWD_{2-1}	Pulse Width Distortion $\lvert t_{PLH2-1} - t_{PHL2-1} \rvert$				34	135	ns

12. ESD Ratings and V_{ISO}

PARAMETER		TEST CONDITIONS		VALUE S	VALUE G	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pins	±8000	±8000	V
			All pins	±4000	±4000	
		Charged-device model (CDM), per JEDEC specification		±2000	±2000	
		Machine Model JEDEC JESD22-A115-A, all pins		±200	±200	
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 2500 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 3000 V_{RMS}, t = 1 s (100% production)		3750	5000	V_{RMS}

13. Parameter Measurement Information



- **Test Circuit of SiS154x**

14. Typical Application

The SiS1540 and SiS1541 isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, eliminating ground loops. These devices do not require special power-supply sequencing, the logic levels are set independently on either side by Vcc1 and Vcc2. The SDA1, SCL1, SDA2, SCL2 pins have open-drain outputs, requiring pull-up resistors to their respective supplies for logic-high outputs. The output low voltages are guaranteed for sink currents of up to 35mA for side B, and 3.5mA for side 1. So the minimum pullup resistors on the input lines must be selected in such a way that input current drawn is ≤ 3.5mA on side 1 and output current drawn is ≤ 35mA on side B. The maximum pull-up resistors on the input lines and output lines depend on the load and rise time requirements on the respective lines. To reduce ripple and the chance of introducing data errors, bypass Vcc1 and Vcc2 with at least 0.1µF low-ESR ceramic capacitors to GND1 and GND2 respectively. Place the bypass capacitors as close to the power supply input pins as possible.

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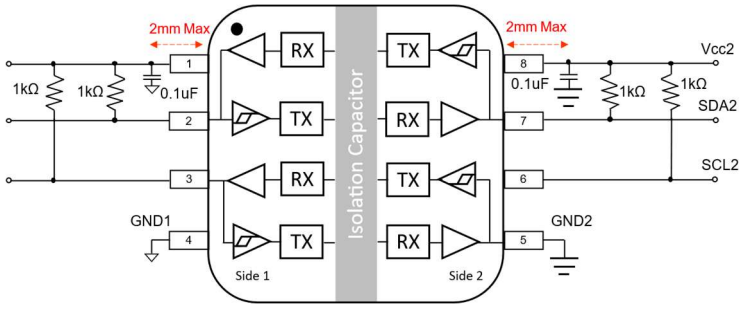
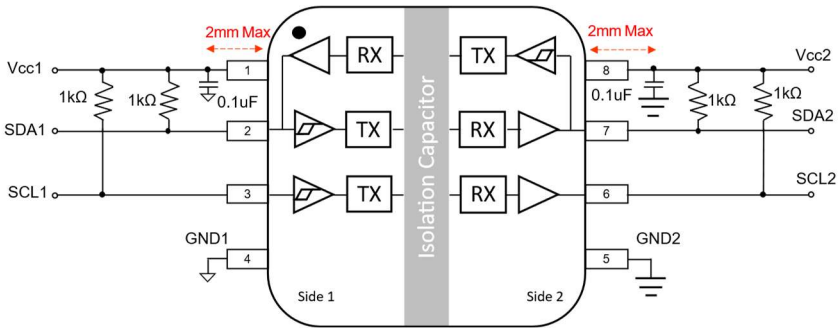
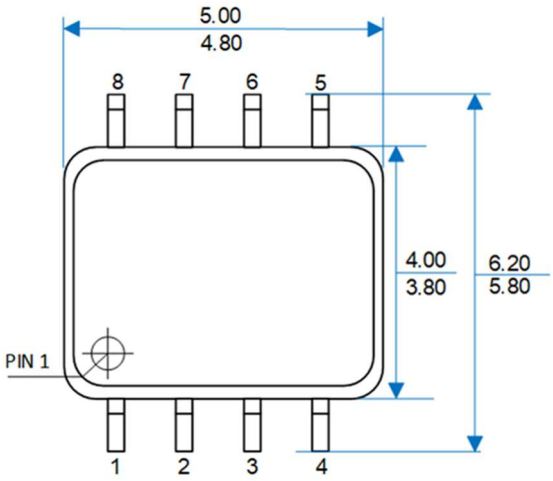


- **Typical Application Circuit of SiS1540**

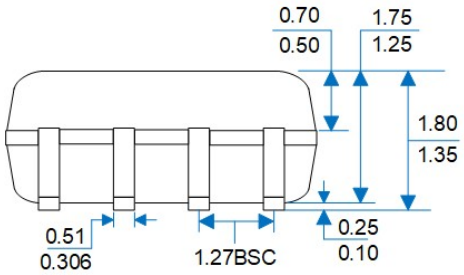


- **Typical Application Circuit of SiS1541**

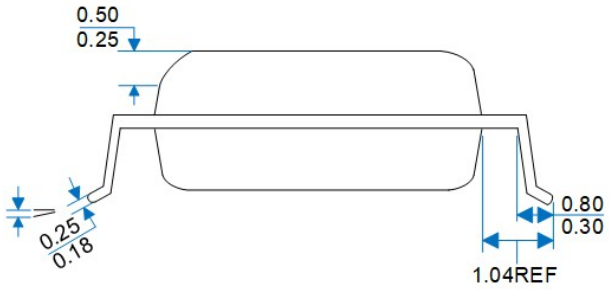
15. Package Outlines: SOP8



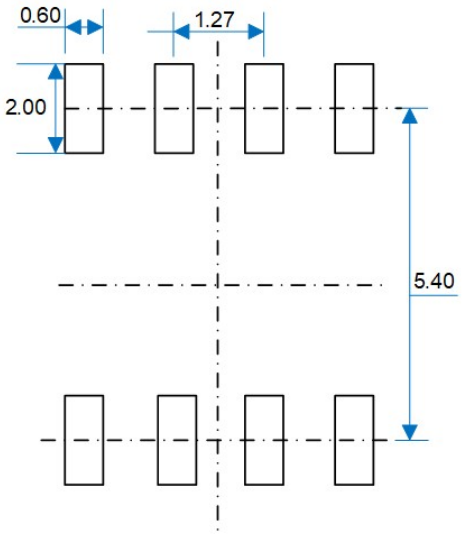
Top View



Side View 1

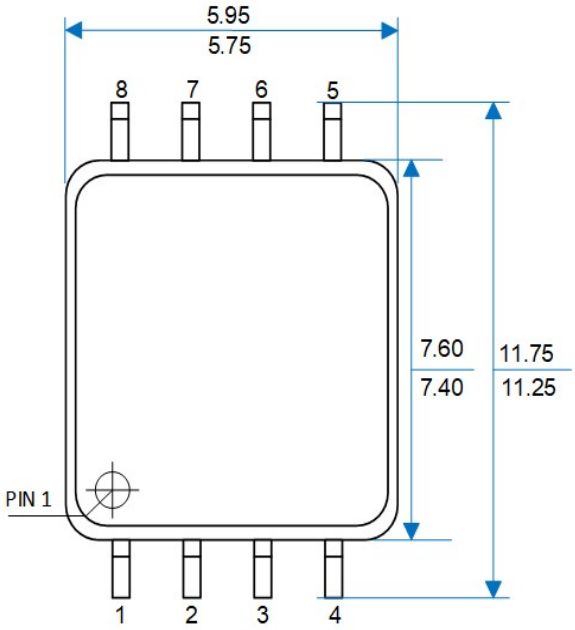


Side View 2

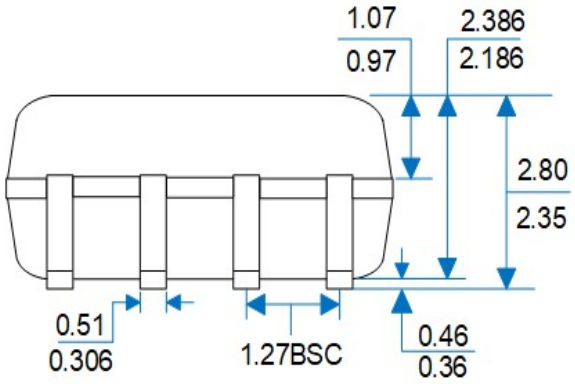


Recommended Land Pattern

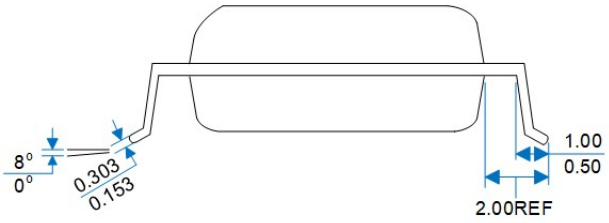
16. Package Outlines: SOW8



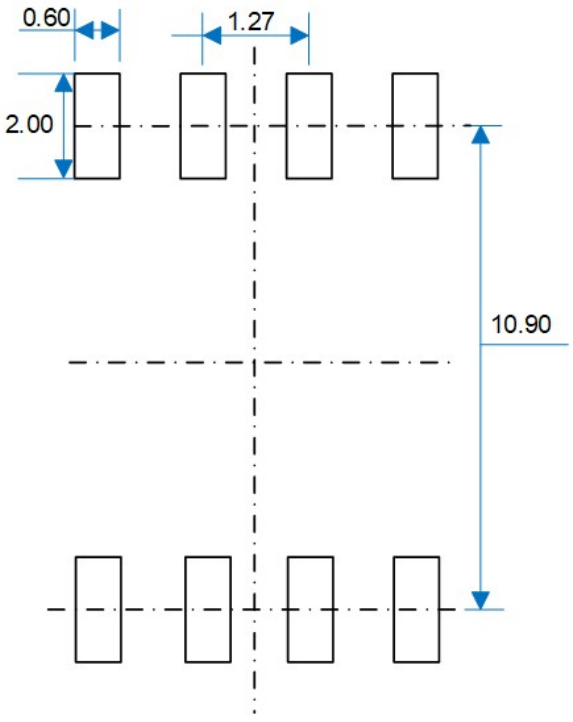
Top View



Side View 1



Side View 2



Recommended Land Pattern

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